

What is claimed is:

1. A semiconductor testing circuit for performing a test of at least one of a write operation and a read 5 operation of a semiconductor storage device, comprising:

a plurality of counters which designate a plurality of different portions of an address signal used in said at least one of the write operation and the read operation, each of the plurality of different portions 10 comprising one bit or a plurality of successive bits; and

a switching circuit which selectively outputs counter-control signals for individually controlling operations of said plurality of counters, where each of said counter-control signals is one of a common counter- 15 control signal commonly used for said plurality of counters and the most significant bit of one of said plurality of portions outputted from a first one of said plurality of counters other than a second one of said plurality of counters for which said each of said counter- 20 control signals is outputted.

2. The semiconductor testing circuit according to claim 1, wherein said switching circuit outputs said common counter-control signal to one of said plurality of counters, and said most significant bit to each of another 25 or others of said plurality of counters.

3. The semiconductor testing circuit according to
claim 1, wherein said switching circuit comprises a
plurality of individual switching circuits which are
respectively provided in correspondence with said
5 plurality of counters, and said counter-control signals
are outputted from the plurality of individual switching
circuits corresponding to said plurality of counters,
respectively.

10 4. The semiconductor testing circuit according to
claim 1, wherein a first one of said plurality of counters
designates a column address of said semiconductor storage
device, and a second one of said plurality of counters
designates a row address of said semiconductor storage
15 device.

5. The semiconductor testing circuit according to
claim 4, wherein said first one of said plurality of
counters is realized by a synchronous counter, and said
20 second one of said plurality of counters is realized by an
asynchronous counter.

6. The semiconductor testing circuit according to
claim 4, wherein a third one of said plurality of counters
25 designates a bank address of said semiconductor storage
device.

7. The semiconductor testing circuit according to
claim 1, wherein one of said plurality of counters
comprises,

an asynchronous counter,

5 a synchronous counter having an output the most
significant bit of which is inputted into said switching
circuit, and

10 a counter selection circuit which receives one
of said counter-control signals outputted for said one of
said plurality of counters, selectively outputs the
received one of the counter-control signals to one of said
asynchronous counter and said synchronous counter,
selectively receives a count value outputted from said one
of the asynchronous counter and the synchronous counter,
15 and outputs the received count value as one of said
plurality of portions designated by said one of said
plurality of counters.

8. The semiconductor testing circuit according to
20 claim 7, wherein said counter selection circuit selects
said synchronous counter as a destination to which the
counter selection circuit outputs the received one of the
counter-control signals and a source from which the
counter selection circuit receives said count value, when
25 said at least one of the write operation and the read
operation is performed.

9. The semiconductor testing circuit according to
claim 7, wherein said one of the plurality of portions
designated by said one of said plurality of counters
designates a bank address of said semiconductor storage
5 device.

10. A semiconductor chip comprising:
a semiconductor storage device; and
a self-testing circuit for performing a
test of at least one of a write operation and a read
operation of a semiconductor storage device;
said self-testing circuit includes,
a plurality of counters which
designate a plurality of different portions of an address
15 signal used in said at least one of the write operation
and the read operation, each of the plurality of different
portions comprising one bit or a plurality of successive
bits, and
a switching circuit which
20 selectively outputs counter-control signals for
individually controlling operations of said plurality of
counters, where each of said counter-control signals is
one of a common counter-control signal commonly used for
said plurality of counters and the most significant bit of
25 one of said plurality of portions outputted from a first
one of said plurality of counters other than a second one
of said plurality of counters for which said each of said

counter-control signals is outputted.

11. A packaged semiconductor device comprising:

a semiconductor storage device;

5 a self-testing circuit which performs a test of at least one of a write operation and a read operation of a semiconductor storage device; and

a package in which said semiconductor storage device and said self-testing circuit are packed;

10 said self-testing circuit includes,

a plurality of counters which designate a plurality of different portions of an address signal used in said at least one of the write operation and the read operation, each of the plurality of portions comprising one bit or a plurality of successive bits, and

a switching circuit which selectively outputs counter-control signals for individually controlling operations of said plurality of counters, where each of said counter-control signals is one of a common counter-control signal commonly used for said plurality of counters and the most significant bit of one of said plurality of portions outputted from a first one of said plurality of counters other than a second one of said plurality of counters for which said each of said counter-control signals is outputted.

12. A semiconductor storage device comprising:

memory cells; and

a self-testing circuit which performs a test of at least one of a write operation and a read operation in said memory cells;

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said self-testing circuit includes,

a plurality of counters which designate a plurality of portions of an address signal used in said at least one of the write operation and the read operation, by count values outputted from the 10 plurality of counters, respectively, where each of the plurality of portions is comprised of one bit or a plurality of successive bits, and

a switching circuit which selectively outputs counter-control signals for 15 individually controlling operations of said plurality of counters, where each of said counter-control signals is one of a common counter-control signal commonly used for said plurality of counters and the most significant bit of one of said plurality of portions outputted from a first 20 one of said plurality of counters other than a second one of said plurality of counters for which said each of said counter-control signals is outputted.

13. The semiconductor storage device according to 25 claim 12, wherein said switching circuit outputs said common counter-control signal to one of said plurality of counters, and said most significant bit to each of another

or others of said plurality of counters.

14. The semiconductor storage device according to
claim 12, wherein said memory cells are arranged in a
5 plurality of banks, which can be designated by said
address signal, and the plurality of banks share a data
bus through which data are written in or read from said
memory cells.

10 15. A semiconductor testing method for performing a
test of at least one of a write operation and a read
operation of a semiconductor storage device, comprising
the steps of:

(a) selectively inputting counter-control
15 signals into a plurality of counters so as to individually
control counting operations of the plurality of counters,
where each of the counter-control signals is one of the
most significant bit of an output of a first one of the
plurality of counters other than a second one of the
20 plurality of counters to which said each of the counter-
control signals is inputted and a common counter-control
signal which is commonly used for said plurality of
counters; and

(b) designating one bit or a plurality of
25 successive bits constituting an address signal used in
said at least one of the write operation and the read
operation, by each of count values outputted from the

plurality of counters.

16. The semiconductor testing method according to
claim 15, wherein said common counter-control signal is
5 inputted into one of said plurality of counters, and said
most significant bit is inputted into each of another or
others of said plurality of counters.

17. The semiconductor testing method according to
10 claim 15, wherein a column address is designated by a
count value outputted from one of the plurality of
counters to which said common counter-control signal is
inputted, so as to perform said at least one of the write
operation and the read operation in a page mode.

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18. The semiconductor testing method according to
claim 15, wherein a bank address is designated by a count
value outputted from one of the plurality of counters to
which said common counter-control signal is inputted, so
20 as to perform said at least one of the write operation and
the read operation in a bank-interleave mode.